



# New Tools and Standards Boost Embedded Systems Performance

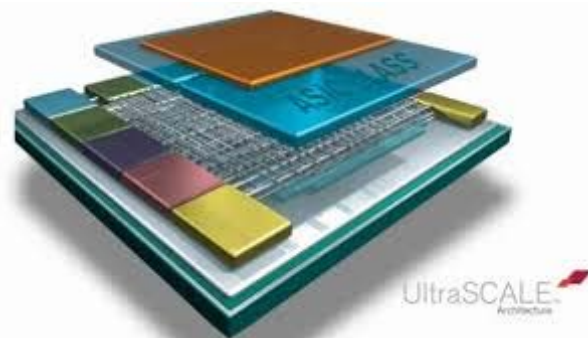
*Rodger Hosking  
Pentek, Inc.*

*Embedded Tech Trends  
January 2017*



# Topics

- New Challenges for Real-time Embedded Systems
- Evolving Xilinx FPGA Technology
- JESD204B Gigabit Serial Peripheral Interfaces
- AXI4 Interconnect Standard
- Navigator Design Tools





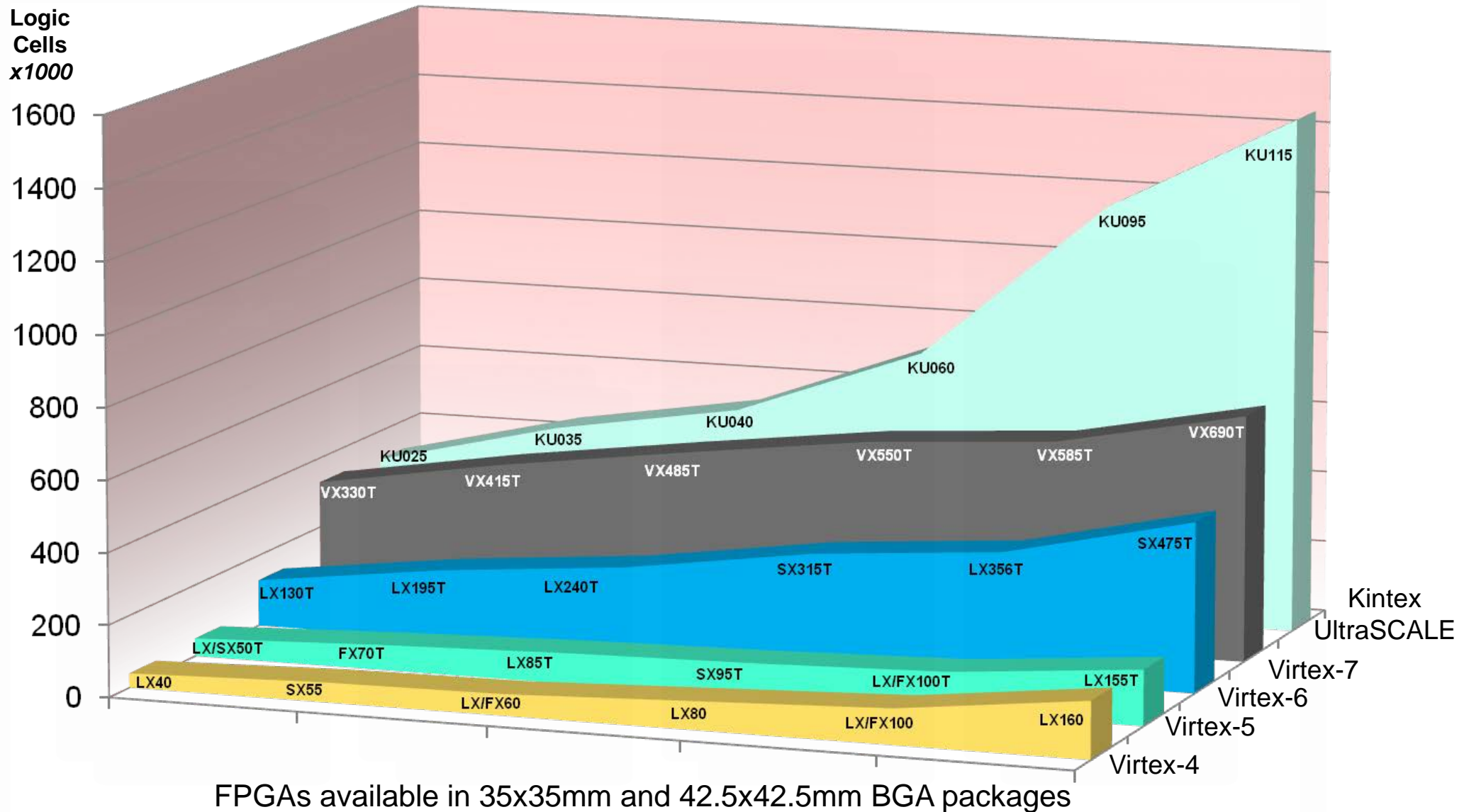
# Challenges for Real-Time Embedded Systems

- Increased Component Density
- Higher Device Complexity
- Higher-Speed Data Converters
- Faster Device and Board Interfaces
- Longer Development Cycles
- New Technology Insertion
- Design Portability
- Reliability and Maintainability
- Life Cycle Management
- SWaP-C

- New Device Technology
  - Geometry and process improvements
- Faster Interconnect Technology
  - Migration to gigabit serial links
- Open Hardware Standards
  - Boards, Backplanes, & Chassis
  - Links, Protocols & Interfaces
- Open FPGA Standards
  - HDL & Module Interfaces
- Graphically Oriented Design Tools
  - Block Diagram Design Entry
- High-Level Software Tools
  - API with Layered Modules

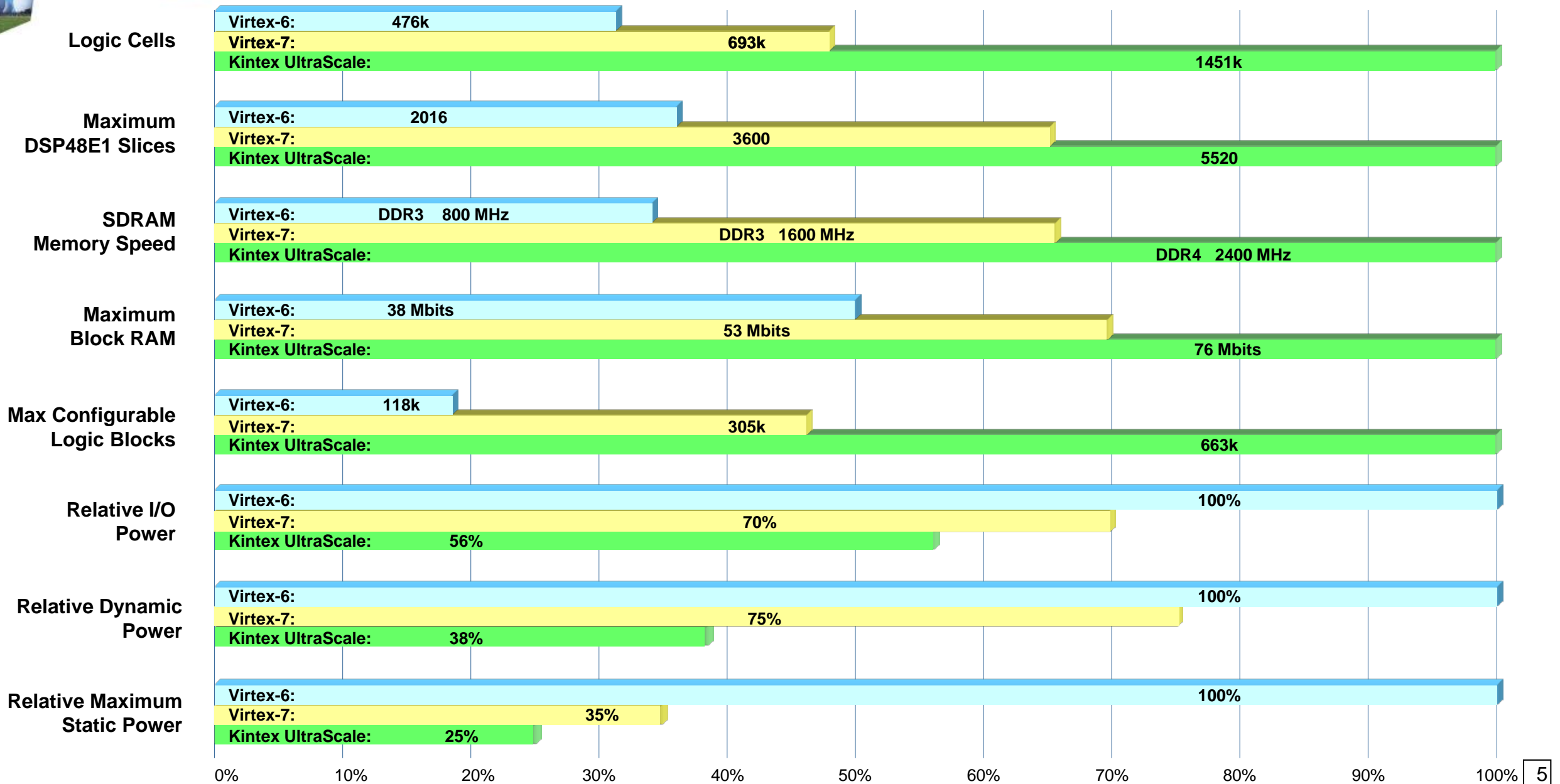


# Evolution of Xilinx FPGA Series





# Comparing Virtex-6, Virtex-7, & Kintex UltraScale





# Virtex-6, Virtex-7 & Kintex UltraScale Comparisons



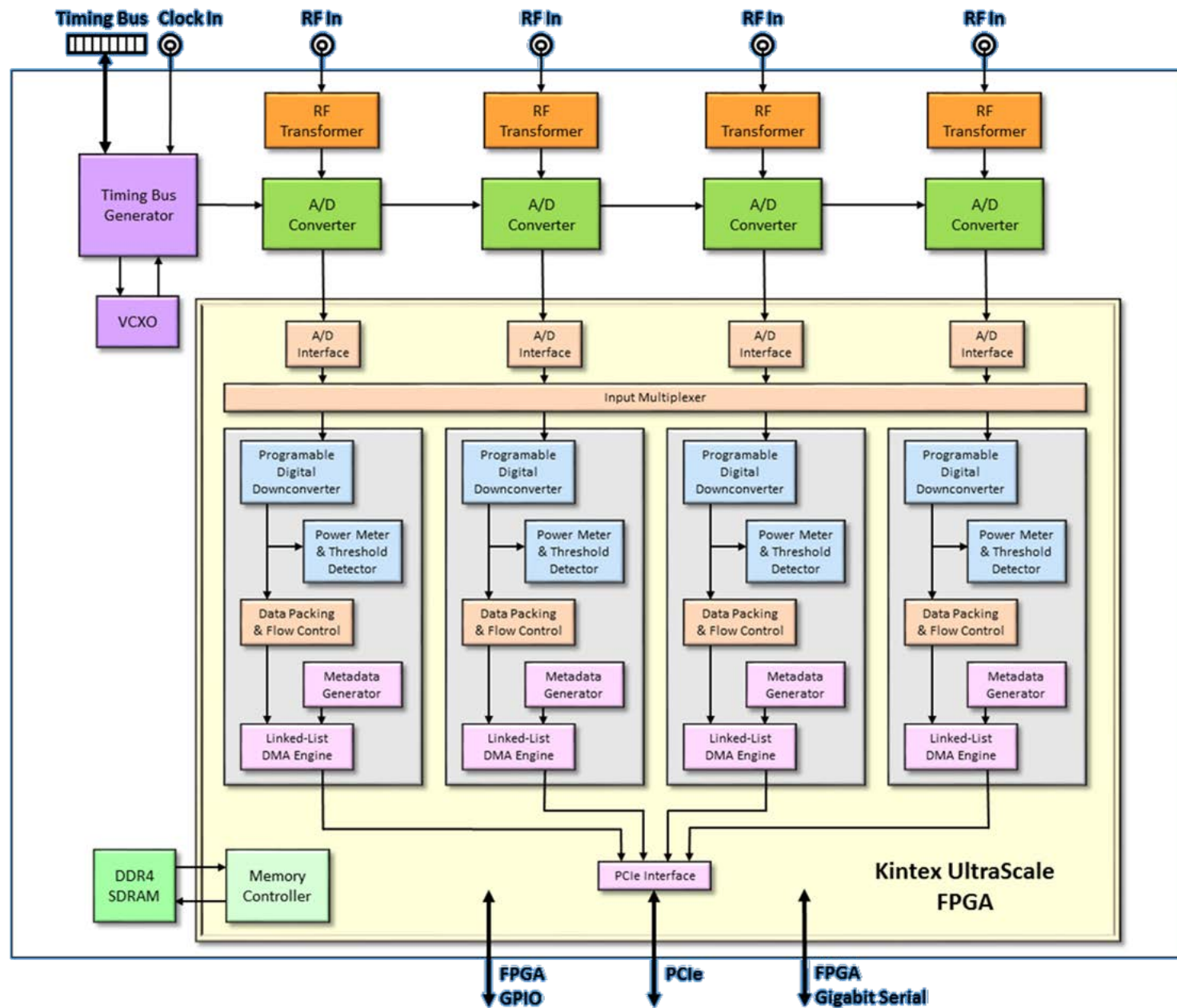
	Virtex-6			Virtex-7		Kintex UltraScale		
	LX130	LX240	SX315	VX330	VX690	KU035	KU060	KU115
Logic Cells	128K	241K	314K	326K	693K	444K	726K	1451K
DSP slices	480	768	1344	1120	3600	1700	2760	5520

- Excellent range of FPGA resources for the same XMC I/O function
  - Scalable by more than a factor of 10
  - Customer can choose the most cost effective solution
  - Eases upgrades and new technology insertion
  - Minimizes life cycle support issues
- Kintex UltraScale Compared with Virtex-6 and Virtex-7
  - Cost per Logic Cell and DSP Slice Reduced by 30% to 50%
  - Power dissipation reduced by 20% to 40%



# Factory Installed FPGA Features Simplify Development

- Acquisition Engines
  - Pre-Triggering & Delayed-Triggering
  - Radar Range Gate Generation
  - Synchronous across boards
- Multiband Digital Downconverters
  - Decimation from 2 to 65K
  - Bandwidths from 80 MHz to 3 kHz
- Real Time Power Meters
  - Energy detection
  - Programmable threshold interrupts
- Metadata Generators
  - Precise Time-stamping
  - Channel ID & block counter
- Linked List DMA Controllers
  - Delivers Data Blocks across PCIe to System Memory





# LVDS Data Converter Interfaces

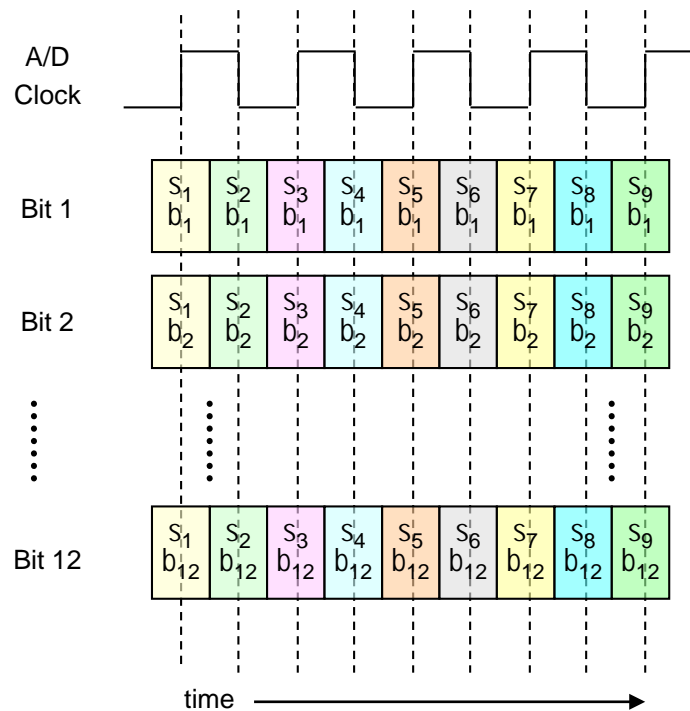
- Traditional Data Converters Use Parallel LVDS I/O
  - Each clock or clock edge transfers one bit for each data sample
  - Data clock and A/D clock are the same – one sample per clock
  - Example: A 12-bit A/D requires one LVDS pair per bit

- Advantages

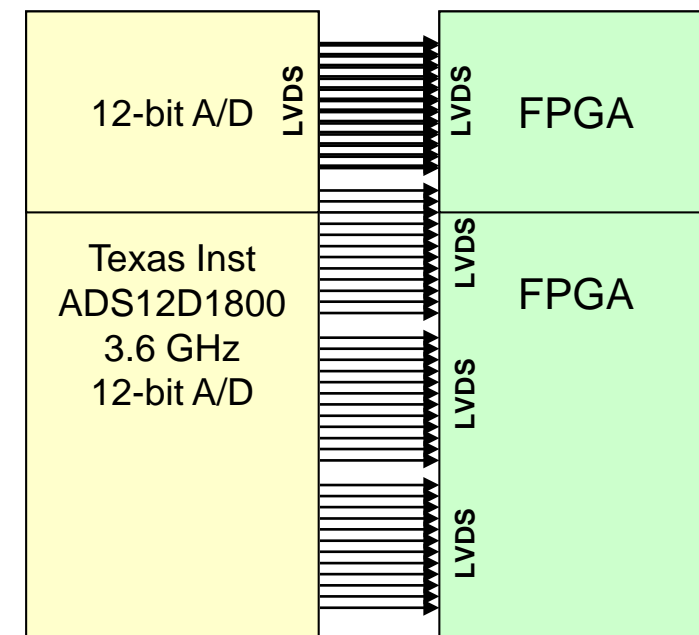
- Simple
- Easy to change sample rate with no changes in the FPGA

- Disadvantages

- Consumes FPGA I/O pins
- Requires many PCB traces - eats up real estate & layers
- High speed data converters need multiple banks of LVDS pairs



**LVDS**  
12 LVDS Pairs  
= 24 PCB traces



**Aggregate Rate: 5.4 GB/sec**





# JEDS204B Gigabit Serial Data Converter Interfaces

## ■ JESD204B Gigabit Serial Interface

- Gigabit serial links up to 12.5 Gbaud
- Different data framing for each mode
- Data scrambler, alignment codes, 8B10B channel coding, idle patterns, etc.

## ■ Advantages

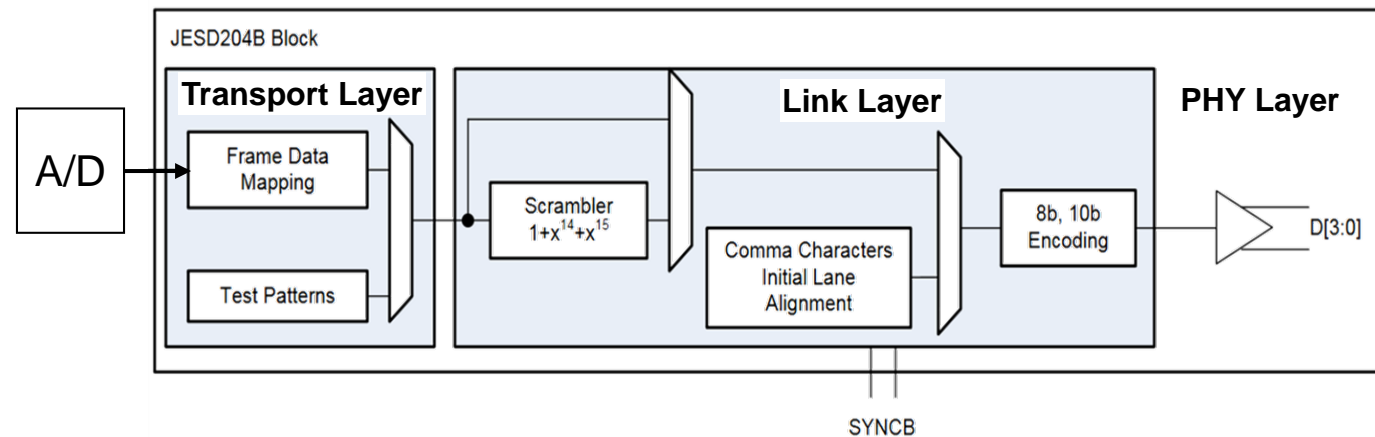
- Far fewer traces, but require strict layout and matching
- Uses native GTX and GTH gigabit serial I/O pins of FPGAs
- Supports higher sample rates, DDCs, and channel counts

## ■ Disadvantages

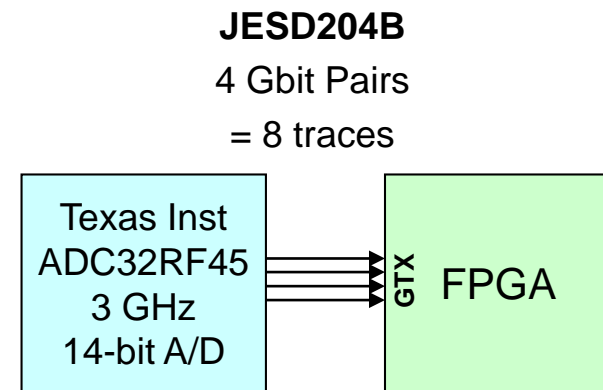
- Many data frame modes including DDC modes with different bandwidths
- Converter sample rate and gigabit serial rates are locked at fixed ratio
- Changing sample rates and modes requires changing JESD204B clock rate of the FPPA JESD204B receivers – inconvenient!

## ■ COTS vendors must abstract these complexities from the user

- Requires extensive investments in software and FPGA tools



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**Aggregate Rate: 5.25 GB/sec**



# AXI-4 Standard – What Is It?

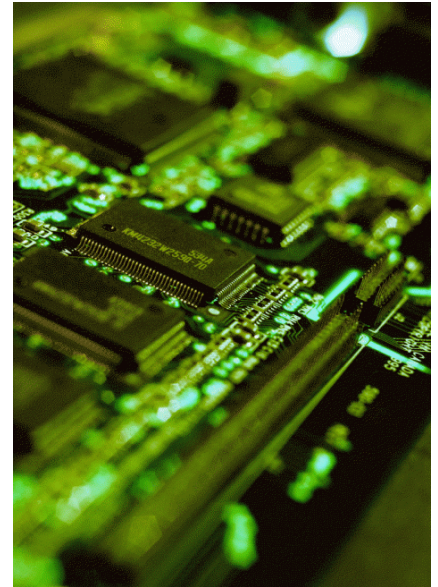
- AXI (Advanced eXtensible Interface) is part of the ARM<sup>®</sup> AMBA<sup>®</sup> (Advanced Microcontroller Bus Architecture)
- It is an open standard, on-chip interconnect specification for functional blocks in SoC (system-on-chip) designs
- The AMBA 4 AXI4 specifications were introduced in 2010
- Due to larger and more complex IP for FPGAs, Xilinx adopted AXI4 as the interface standard for IP blocks to communicate in their Vivado tools
- Now both Xilinx and Altera have embraced AXI4 not only for interconnecting FPGA IP blocks, but also for on-chip processors and peripherals





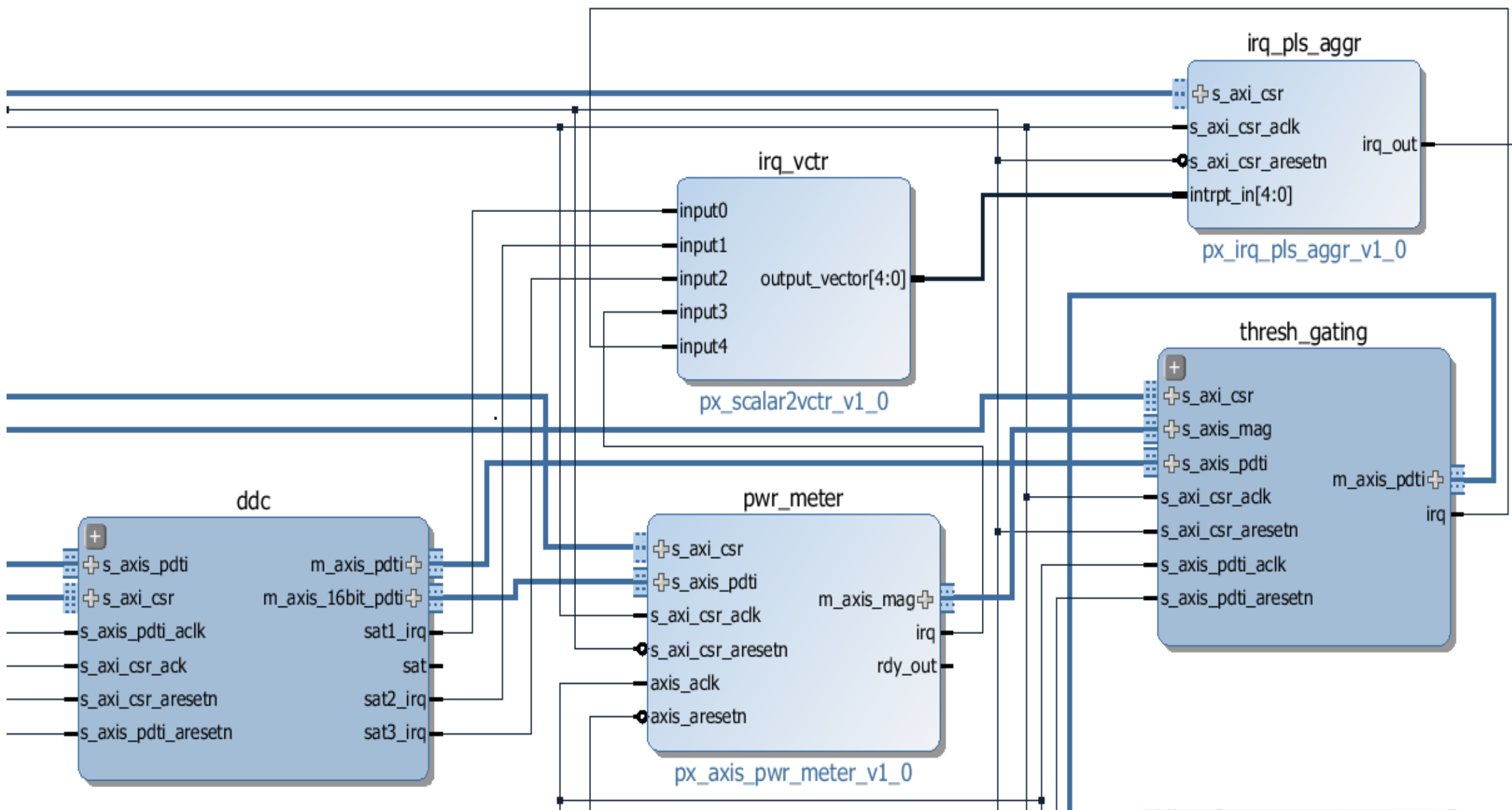
# Why Use AXI4 in FPGAs?

- AXI4 handles much of the “housekeeping” like matching speeds and data widths between blocks
- Customers who follow the AXI4 guidelines when creating custom IP from scratch can expect the IP to connect to existing AXI4 IP
- AXI4 eases integration and interfacing of IP cores from vendors like Xilinx and other third parties with “plug and play” compatibility
- AXI4 abstraction of interconnects simplifies graphically oriented block diagram-type design environments such as the Xilinx IP Integrator
- Entire buses can be abstracted into single “wires.”
- Improves productivity, portability and reusability





# Pentek Navigator IP is delivered as AXI4 Blocks





# Designing IP with VHDL

The screenshot displays the Vivado 2015.2 IDE interface for a project named 'px71860'. The main window is titled 'Block Design - p71860\_infrastructure' and shows a hierarchy of components under 'Synthesis (2183)'. The 'IP Integrator' section is active, showing the 'AXI4-Stream Broadcaster' IP with version 1.1 (Rev. 5). The description states: 'The AXI4-Stream Broadcaster IP provides the ability to replicate one SI stream onto multiple MI stream channels.' The status is 'Pre-Production' and the license is 'Included'. The 'Sources' tab is selected, showing the source file 'p71860\_infrastructure\_axis\_sync\_ram\_broadcaster\_0.xdi'. The 'Log' window at the bottom shows the synthesis process, including parsing XDC files for various components like 'hmc\_intrfc/hmc\_init1/mdm\_0/U0' and 'hmc\_intrfc/hmc\_init1/mdm\_0/U0'. The 'VHDL' editor shows the code for 'p71860.vhd', which includes a process for generating an idelayctrl reset and a port map for the 'IDELAYCTRL' component. The port map defines 'RDY' as an output, 'REFCLK' as a reference clock input, and 'RST' as an active high reset input. The code also defines a 'bufg' component with a port map for 'bufg\_cfg\_spc\_sck' and 'CFG\_SPC\_SCK'.



# Graphical AXI4 IP Design with Xilinx Vivado IP Integrator

**Pentek AXI4 IP**

**Xilinx AXI4 IP**

Block Design - p71860\_infrastructure

Sources

- p71860\_infrastructure (4248)
- Synthesis (2183)
- p71860\_infrastructure\_axis\_sync\_ram\_broadcaster\_0
- p71860\_infrastructure\_axis\_pcie\_rq\_switch\_0 (27)
- p71860\_infrastructure\_axis\_hmc\_rsp\_broadcaster\_0 (1)
- p71860\_infrastructure\_axis\_hmc\_rqst\_switch\_0 (27)
- p71860\_infrastructure\_axis\_misc\_cntl\_broadcaster\_0 (1)
- p71860\_infrastructure\_xlconstant\_0\_0 (2)
- p71860\_infrastructure\_xlconstant\_1\_0 (2)
- p71860\_infrastructure\_xlconcat\_0\_0 (2)
- p71860\_infrastructure\_axis\_sync\_ram\_broadcaster\_1 (1)
- p71860\_infrastructure\_hmc\_rsp\_axis\_broadcaster\_0 (1)
- p71860\_infrastructure\_hmc\_rqst\_axis\_switch\_0 (27)
- p71860\_infrastructure\_axis\_sync\_ram\_broadcaster\_2 (1)
- p71860\_infrastructure\_axis\_hmc\_rsp\_broadcaster\_1 (1)
- p71860\_infrastructure\_axis\_hmc\_rqst\_switch\_1 (27)
- p71860\_infrastructure\_xlconstant\_0\_1 (2)
- p71860\_infrastructure\_xlconstant\_1\_1 (2)
- p71860\_infrastructure\_xlconcat\_0\_1 (2)

Hierarchy IP Sources Libraries Compile Order

Source File Properties

Source File Properties

p71860\_infrastructure\_axis\_sync\_ram\_broadcaster\_0.xci

IP name: AXI4-Stream Broadcaster

Version: 1.1 (Rev. 5)

Interfaces: AXI4-Stream

Description: The AXI4-Stream Broadcaster IP provides the ability to replicate one SI stream onto multiple MI stream channels.

Status: Pre-Production

License: Included

General Properties IP

Messages

3 errors 60 critical warnings 298 warnings 2,092 infos 647 statuses Show All

Implementation (3 errors, 60 critical warnings)

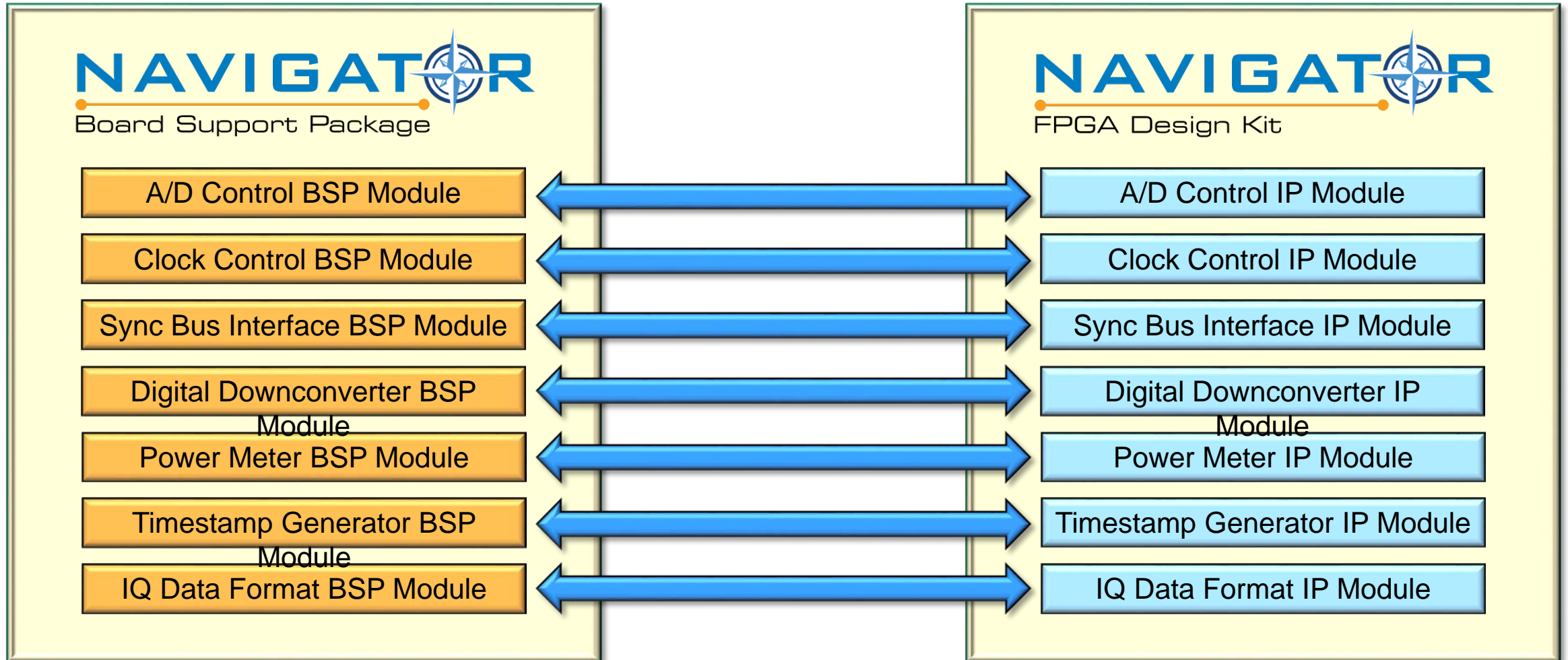
- Design Initialization (60 critical warnings)
- [Common 17-55] 'get\_property' expects at least one object. [px\_test\_siq\_gen\_axidcknv\_docks.xdc:20] (59 more like this)
- Opt Design (3 errors)
- [DRC 23-20] Rule violation (RPF-1) IO port is missing a buffer - Device port VP\_VN\_V\_N should be connected to an IO cell such as an [IO]BUF\*. (1 more like this)
- Vivado: Tcl 4-781 Error(s) found during DRC. Opt. design not run



# NAVIGATOR

Design Suite

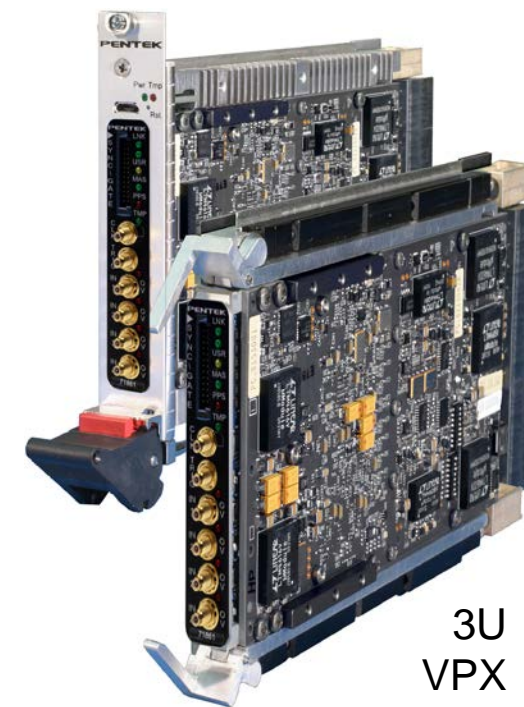
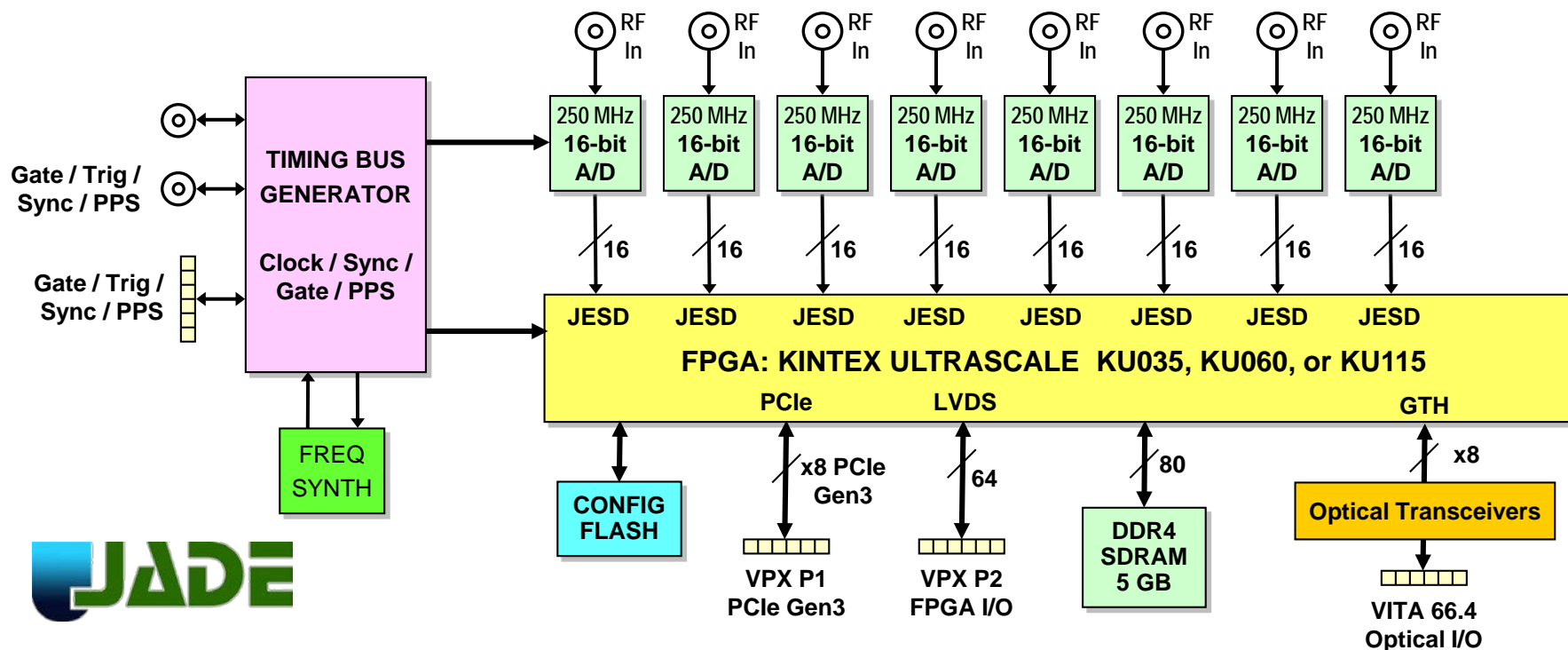
- Direct mapping of BSP API Functions and FPGA IP Modules simplifies software support for customer developed IP





# 52131: 8-Ch 250 MHz 16-bit A/D + DDCs 3U VPX Module

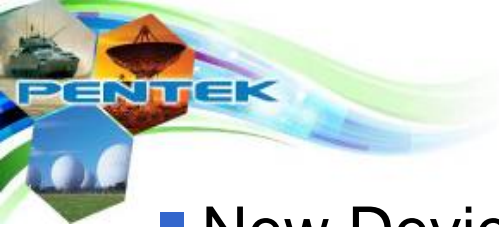
- Kintex UltraScale FPGA
  - KU035, KU060, or KU115
- Eight 250 MHz 16-bit A/Ds
  - Texas Inst ADS42LB69
  - Full 200 MHz Bandwidth
  - JESD204B Interfaces
- Eight Multiband DDCs
  - Decimation from 2 to 64K
- 5 GB DDR4 2400 MHz SDRAM
- VITA 66.4 Optical I/O
  - 8 GB/sec to Backplane
- PCIe Gen 3 x8
- Sample Clock Synthesizer
- Multi-channel Synchronization
- Navigator FPGA Design Kit
- Navigator Board Support API
- Releasing at ETT Show Today!



3U  
VPX







# Solutions for Real-Time Embedded Systems

- **New Device Technology** →
  - Geometry and process improvements
- **Faster Interconnect Technology** →
- **Open Hardware Standards** →
- **Open FPGA Standards** →
- **Graphically Oriented Design Tools** →
- **High-Level Software Tools** →
- **Kintex UltraScale FPGA**
  - More Resources, Lower Power & Cost
- **JESD204B Interconnect Standard**
  - Faster, fewer wires, less space
- **VITA 66.4 Optical Backplane**
  - Blind mating, eliminates front connectors
  - Fast, long distance data links
- **AXI4 IP Interconnects**
  - Graphical design, portability, reusability
- **Xilinx Vivado IP Integrator**
  - Graphically connects AXI4 IP Blocks
- **Pentek Navigator Tool Suite**
  - API Libraries, AXI4 FPGA IP Blocks



Thank You!! – Questions??

